UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,714	11/20/2001	Hiroki Kuribayashi	041465-5127	9135

9629 7590 03/17/2005

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
CHAI, LONGBIT	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,714	KURIBAYASHI ET AL.	
	Examiner	Art Unit	
	Longbit Chai	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/7/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for benefit of foreign priority under 35 U.S.C. 119 (a) – (d) is acknowledged.

2. The application is filed on 11/20/2001 but has a foreign priority application filed on 11/28/2000.

Specification

3. The disclosure is objected to because of the following informalities:

4. The acronym should be defined on the first appearance, especially, for those used in the Abstract such as ECC and RLL. See 37 CFR 1.71. Appropriate correction is required.

Claim Objections

5. Claim 14 is objected to because of the following informalities: "according to claim 1" should be "according to claim 7". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraph of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

6. Claims 1, 6, 7 and 12 – 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsui (Patent Number: 5949750), hereinafter referred to as Matsui.

As per claim 1 and 7, Matsui teaches a data recording method of using random series to scramble input data and generate recording data, comprising:

a random series generation process of generating a pre-determined random series (Matsui: see for example, Figure 4A Element 20 and Column 5 Line 56 – 58);

a random series conversion process of selectively converting said random series to different random series based on recording position data (Matsui: see for example, Figure 3A, 4A / 4B & 5A, Column 5 Line 9 – 30, Column 5 Line 53 – 67, Column 6 Line 11 – 14 and Column 6 Line 47 – 67: the random series conversion process is interpreted as the M period sequence generator rearranged by the sector address signal (Figure 4A) and a predetermined length Dw offset value (Figure 4B) as taught by Matsui); and

a scrambling process of using said converted random series to scramble input data (Matsui: see for example, Figure 4A Element 40).

As per claim 6 and 12, Matsui teaches the claimed invention as described above (see claim 1 and 7 respectively). Matsui further teaches said recording data are recorded in order on tracks on a disk-shaped medium, and in said random series conversion process are converted to different random series for adjacent tracks (Matsui: see for example, Column 6 Line 30 – 40 and Column 8 Line 41 – Column 9 Line 19).

As per claim 13 and 14, Matsui teaches the claimed invention as described above (see claim 1 and 7 respectively). Matsui further teaches descrambling input data by using a random series which; generates reproduction data by using the random series that were selected during scrambling to descramble said input data (Matsui: see for example, Column 10 Line 4 – 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 4, 5, 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui (Patent Number: 5949750), hereinafter referred to as Matsui, in view of Yamawaki (Patent Number: 5987630), hereinafter referred to as Yamawaki.

As per claim 2 and 8, Matsui teaches the claimed invention as described above (see claim 1 and 7 respectively). Matsui further teaches said random series conversion process converts said random series to different random series based on said recording position data (Matsui: see for example, Column 6 Line 51 – 67).

However, Matsui does not disclose expressly said random series conversion process converts said random series to different random series by performing interleaving on said random series by rearranging the bit order of the output bits of said random series.

Yamawaki teaches said random series conversion process converts said random series to different random series by performing interleaving on said random series by rearranging the bit order of the output bits of said random series (Yamawaki: see for example, Column 5 Line 26 – 45, Column 10 Line 39 – 43 and Table I / Column 6 Line 26 – 31: The new bit positions of the random number b8 – b14 is indeed interleaved with the bit position b0 – b6 as shown in Table I / Column 6 Line 26 – 31).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Yamawaki within the system of Matsui because Yamawaki teaches providing a scramble pattern generator suitable for

improving the data transfer rate and fast data processing (Yamawaki: see for example, Column 2 Line 54 – 58).

Accordingly, Matsui in view of Yamawaki teaches said random series conversion process converts said random series to different random series by performing interleaving on said random series by rearranging the bit order of the output bits of said random series based on said recording position data.

As per claim 4 and 10, Matsui teaches the claimed invention as described above (see claim 1 and 7 respectively). Matsui further teaches performing said random series conversion process based on said recording position data, and then performs a delayed output of that random series and converts said random series to different random series based on the results of the performed calculation (Matsui: see for example, Figure 4A / 4B & 5A, Column 5 Line 53 – 67, Column 6 Line 11 – 14 and Column 6 Line 47 – 67).

However, Matsui does not disclose expressly said random series conversion process performs interleaving on said random series by rearranging the bit order of the output bits of said random series.

Yamawaki teaches said random series conversion process performs interleaving on said random series by rearranging the bit order of the output bits of said random series (Yamawaki: see for example, Column 5 Line 26 – 45, Column 10 Line 39 – 43 and Table I / Column 6 Line 26 – 31: The new bit positions of the random number b8 – b14 is indeed interleaved with the bit position b0 – b6 as shown in Table I / Column 6 Line 26 – 31).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Yamawaki within the system of Matsui because Yamawaki teaches providing a scramble pattern generator suitable for improving the data transfer rate and fast data processing (Yamawaki: see for example, Column 2 Line 54 – 58).

Accordingly, Matsui in view of Yamawaki teaches said random series conversion process performs interleaving on said random series by rearranging the bit order of the output bits of said random series based on said recording position data, and then performs a specified calculation on the interleave random series and delayed output of that random series and converts said random series to different random series based on the results of the performed calculation.

As per claim 5 and 11, Matsui teaches the claimed invention as described above (see claim 2 and 8 respectively). Matsui further teaches said random series conversion process performs said interleaving on a 16-bit random series (Matsui: see for example, Column 7 Line 29 – 30).

Yamawaki further teaches alternately selects and outputs the high-order 8 bits or low-order 8 bits (Yamawaki: see for example, Column 5 Line 26 – 45 & Table I / Column 6 Line 26 – 31: Yamawaki teaches the selector selects the initial scramble pattern in response to the L-level select signal SL, which is evident the initial scramble pattern is mapped to the high-order bits as shown in able I / Column 6 Line 26 – 31. In addition, Yamawaki also teaches the selector selects the new scramble pattern in response to

the H-level select signal SL and it is evident that the new scramble pattern is mapped to the low-order bits as shown in able I / Column 6 Line 32 – 38).

Accordingly, in view of Yamawaki teaches said random series conversion process performs said interleaving on a 16-bit random series, then alternately selects and outputs the high-order 8 bits or low-order 8 bits.

8. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui (Patent Number: 5949750), hereinafter referred to as Matsui, in view of Ibaraki (Patent Number: 5546461), hereinafter referred to as Ibaraki.

As per claim 3 and 9, Matsui teaches the claimed invention as described above (see claim 1 and 7 respectively). Matsui further teaches said random series conversion process converts said random series to different random series based on said recording position data (Matsui: see for example, Column 6 Line 51 – 67).

However, Matsui does not disclose expressly said random series conversion process converts said random series to different random series by inverting the bits of said random series according to an inverted pattern.

Ibaraki teaches said random series conversion process converts said random series to different random series by inverting the bits of said random series according to an inverted pattern (Ibaraki: see for example, Column 20 Line 6 – 13).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Ibaraki within the system of Matsui

because Ibaraki teaches providing a scramble / descramble apparatus capable correctly and effectively executing a scramble process and not allowing the original video signal to be obtained from the scrambled video signal (Ibaraki: see for example, Column 3 Line 14 – 16).

Accordingly, Matsui in view of Ibaraki teaches said random series conversion process converts said random series to different random series by inverting the bits of said random series according to an inverted pattern based on said recording position data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Longbit Chai whose telephone number is 571-272-3788. The examiner can normally be reached on Monday-Friday 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Longbit Chai
Examiner
Art Unit 2131

LBC

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100